VXI Model VX2805C

8 Channel Data Acquisition Module

Heritage

The VX2805C is a fourth generation COTS product. The predecessors to this module, interfaced with IMPAX software (also COTS), have been used to accurately characterize initial dynamics for launch vehicles such as Titan, as the "turn-key" Lift Off Instrumentation System (LISA). The VX2805C is being used in a prestigious shock laboratory for research and validation of state of the art accelerometers, and at the world's largest automotive airbag manufacturer, for the development and testing of air bags.

Description

The Model VX2805C is a completely integrated 8 channel data recording VXI module. Each channel includes a bridge signal conditioner, a low pass filter, a 16-bit 5M Samples/sec/ch ADC, and 16M Samples of DRAM storage per channel. DRAM may be divided into 2, 4 or 8 segments for multiple event recording.

Built-in channel conditioning is suitable for strain gauge bridge-type transducers and for voltage signals. Constant voltage excitation is independently programmable for each channel. Special function signal conditioning requirements may be accommodated with SIPS™ (Smart Interface Panel System) product families and controlled by the VX2805C onboard processor.

Highlights

- o 8 Channels Per Module
- o Each Channel Includes Signal Conditioning, Filter, ADC and Memory
- o 16-Bit Resolution
- o High Dynamic Range
- o Up to 5M Samples/s/ch
- o Simultaneous Sampling
- o Dual Ported Memory Access at Rates <5M S/s
- o 1k Snapshot Data FIFO for Each Channel
- o 2.3MHz 3dB Bandwidth
- o Buffered Analog Output for Each Channel
- o Overload Detection for Each Channel
- o Excellent Ch-to-Ch Phase Match
- o Computer Controlled Calibration
- o 16M Samples Storage per Channel
- o Multi-Event Recording
- o Digital Signal Processors
- o Digital Filters, Flat Passband, Sharp Cutoff
- o Internal and External Triggering
- o Pre- and Post-Trigger Recording
- o Gated Mode
- o Dual Clock Rate Data Recording
- o Constant Voltage Excitation
- o SIPS™ Communication Port
- o Fully Programmable
- o Memory Battery Backup Capability
- o Single Width, C-size, VXI Module
- o Simple Multi-Chassis Phase Clk & Triggering
- o Permits Multiple Chassis Expansion/Operation
- o ECL Clock & Trigger Capabilities

Input full-scale sensitivity is programmable from ±10mV to ±5V in 3dB steps. A 16-bit ADC provides high accuracy, a high dynamic range and resolutions from 340nV to 170µV per count. Offset correction range is ±2.5V with 16-bit resolution. A dedicated signal processor provides superb digital filtering. Filter Fco auto-tracks the sample rate, plus custom filter download capabilities. Dedicated hardware may generate a trigger from the analog signal being digitized on Channel #1 using either level and slope, or window criteria. Trigger Holdoff may be invoked to reject threshold crossings of short duration. Holdoff may improve triggering reliability under noisy signal conditions.

The VX2805C auto bridge balance function may be initiated by computer command. A complete end-to-end calibration of each channel, including the transducer, may be performed by a computer calibration routine. You may use either switched or external calibration resistors (with SIPS™) or the unique internal shunt emulation circuit. The shunt emulation technique provides a fast, multi-point calibration check without operator intervention.

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SPECTRAL DYNAMICS

System Specifications VX2805C

SIGNAL INPUT

Type:	Differential
Connection:	8 wires plus shield per 15 pin "D"
Connector Type:	"D" style 15-pin
Input Impedance:	2MW differential, 1MW to ground
Full Scale Ranges:	±10mV to ±5V programmable with 3dB (50%) steps, 19 ranges
Accuracy After Autocalibration:	±0.1% of full scale ±50µV
Gain Temp Coeff:	<0.025%/ C
Offset Temp Coeff:	<0.02%/ C
Linearity:	±0.05% of full scale
Bandwidth:	dc -1.0MHz ±0.1dB at 2.5MHz dc -2.3MHz +0, -3dB at 5MHz
CMRR dc -100Hz:	80dB, ±500mV to ±5V 90dB for full scales <±500mV
CM Voltage Range:	±10V including signal
Crosstalk:	>90dB isolation ch-to-ch
Noise:	20nV/rootHz + 4 counts RMS
Protection:	Buffered ±15V clamp Max 1A for 2µs, 35V DC

ANALOG OUTPUT

An auxiliary analog output is available at the front panel from each channel. The level is ±1V into 50 ohms for a ± full scale signal.

FUNCTIONS

Offset Control: ±2.5V 16-bit resolution

Offset Zero: An Autozero routine built into the VX2805C will set the ADC output to zero using the offset DACs. Autozero is intended for use with voltage type input signals. Autozero may be initiated by computer command.

Bridge Conditioning: 4 wires plus shield, 4 arm bridge devices when used with PIPS.™ 8 wires plus shield, programmable 1, 2 or 4 active bridge arms when used with SIPS.™

Bridge Balance: When a bridge type transducer is used, an auto bridge balance routine controlled by the VX2805C processor will set the ADC output to zero using the 16-bit balance DAC. Range is ±1mA times bridge resistance ±10mV. Auto Bridge Balance may be initiated by computer command.

OVERLOAD DETECTION

Automatic overload detection and reporting for each channel.

SOURCE SELECTION

Software controlled input selection is provided. Selections include external transducer, internal and external reference sources, internal short to ground and ± excitation voltage. A low thermal EMF relay selects between the signal and other inputs. The source for the calibration bus is then independently selectable as internal reference, short to ground or external calibration source.

EXCITATION

Constant Voltage: 0 to ±10V (20V between the plus and minus excite terminals), programmable with 12-bit resolution. Over-current protection. After power up selftest, excitation is normally zero to protect connected transducers. All channels of excitation may be shut-off by a single software command.

SIPS™ Drive: Used for constant current,constant voltage extended current drive capabilities.

ADC

Simultaneous Sampling: Individual 16-bit Sigma-Delta ADC per channel. An array of VX2805Cs may be configured for synchronized simultaneous sampling. Master/Slave clocking is accomplished via VXI Local Bus.

CLOCK

Internal: 5M to 1.25k samples/s/ch, programmable with tracking filter. Clock step "1, 2, 5" style.

External: Has phase-lock clock input and output ports for synchronization of multiple chassis of SD VXI Modules.

DUAL CLOCK RATE DATA COLLECTION

During acquisition of data may be sub-sampled at an integer sub-multiple from 2 to 256 to reduce data volume when high resolution is not required. Sub-sampling is controlled via the external trigger input connector. Tag RAM keeps track of transitions for correct readout indexing.

GATED MODE FOR BURST RECORDING

When gate/trigger input is high, data is collected at specific rate. When gate signal is low, data collection is suspended. Tag RAM keeps track of transitions for readout indexing.

SUPPORTS BANDWIDTH LICENSING (BWL)

The maximum sample rate of individual SD VXI modules can be licensed to fit your budget. Additional bandwidth may be purchased later and is field upgradeable.

FILTERS

Description: The VX2805C uses 3 levels of filtering; analog, digital within ADC, and digital within the signal processors. A Sigma-Delta type ADC over-samples the input signal by a factor of 8 times the maximum sample rate, then integrates and digitally filters the data. It is this over-sampling rate thatdetermines the aliasing frequency of the ADC, which is 20MHz. The ADC is preceded by an analog filter resulting 90dB attenuation at 20MHz.

The ADC has multiple FIR filters providing flat response to1.01MHz and >85dB attenuation above 1.49MHz. The DC to1MHz pass band ripple is <0.01% of full scale at 2.5M sample/s. -3dB at 2.3MHz >82dB at 3.2MHz at 5M sample/s. Dedicated signal processors reduce the ADC data to the required sampling rate and performs digital filtering which tracks that sampling rate.

Filter Characteristics:

Sample rate Sa/s	Pass band Hz	Rejection band Hz	Atten. dB
5.0M	2.3M	3.2M	>82
2.5M	1M	1.56M	85
1.25M	500k	780k	95
500k	200k	312k	95
250k	100k	156k	>100
125k	50k	78k	>100
50k	20k	31.2k	>100
25k	10k	15.6k	>100
12.5k	5k	7.8k	>100
5k	2k	3.12k	>100
2.5k	1k	1.56k	>100
1.25k	500	780	>100

SNAPSHOT FIFO

There are 1k sample programmable length, synchronized parallel load data FIFOs for each channel. All FIFOs in the system may be triggered in parallel for a snapshot in time. This allows phase synchronous, near real-time monitoring for off-board processing.

DATA READOUT

There are 2 readout modes:

1. Direct DRAM Readout one channel at a time via VXI 16-bit data register.
2. Direct DRAM Readout two channels at a time via VXI 32-bit data register.

TRIGGER

There are 5 stop trigger sources:

1. Software Trigger: The VX2805C may be triggered by a VME command.

2. Data Flow Trigger: The VX2805C may be triggered when the channel #1 ADC output (a 16-bit digital value) satisfies programmable 16-bit criteria; slope and level of amplitude window.

Level: ± full scale;

Slope: Positive, Negative;

Window: Trigger when signal amplitude crosses upper or lower boundary of a window. Boundaries programmable to ± full scale in one count increments.

3. External Trigger: The VX2805C may be triggered by a TTL pulse received at the front panel Trig Input.

4. Real Time Trigger: The VX2805C may be triggered when the analog input signal on channel #1 reaches and remains at or above a programmable threshold for a programmable number of samples. Threshold: ± full scale, 12-bit resolution.

5. Backplane Trigger: TTL or ECL.

Trigger Holdoff: When enabled, the signal must remain over threshold for a programable number of 100ms time intervals (up to 255) to qualify as a trigger condition. Holdoff greatly reduces susceptibility to false triggers that could be caused by noise on the signal input line.

Trigger Output: Any of the trigger sources may also be programmed to produce a pulse or level at the front panel TRIG OUT connector to trigger an external device.

Latching Mode: When enabled and triggered, the latching mode will hold the TRIG OUT high, regardless of subsequent changes in the signal amplitude. If the latching mode is not enabled, the TRIG OUT will go from low to high, back to low, etc., depending on the changes in the signal amplitude compared to the programmed threshold.

System Triggering: A trigger pulse is also generated on the VXI Local Bus to simultaneously trigger multiple VX2805C modules. There are 6 selectable trigger lines for group triggering.

Veto: Data acquisition may be started with the trigger vetoed (disabled) to avoid premature triggering. A subsequent VME command will enable the trigger system.

MEMORY

Size: 16M Samples per channel.

Dual Port/Time Sliced Memory Access: Memory may be used as a16M FIFO for extended run applications at rates <5M Sample/s.

Active Memory: User may define amount of active memory used during acquisition for data storage in 1k Sample increments/ch, when shorter record lengths are needed. All channels have the same record length.

Organization: Programmable in 1k Sample blocks between pre-and post-event memory segments for transient recording. All channels have the same segmentation, and pre-and post-trigger ratios.

Battery Backup: Digitized data stored in memory may be protected against power interruptions by connecting an external UPS to the +5V STBY bus, capable of sourcing ˜80mA @5VDC per SD VXI Module or use SD Battery Backup Model TRAPS1-VXI.

Type: Dynamic RAM.

CALIBRATION

Bridge Voltage Insertion: A precision 10kW resistor may be connected to either signal arm of the bridge and is driven by a 16-bit programmable bi-polar voltage source. Current flows of different values are injected into either side of the bridge to simulate multiple shunt resistors. This Digital Transducer Calibrator provides a high resolution, multi-point calibration.

Shunt Calibration: Accomplished with SIPS.™

Gain Calibration: Internal multiple precision voltage references are used by the Model VX2805C processor and firmware to report full scale voltage with 0.1% accuracy.

Programmable Internal Reference: 16-bit DAC for multipoint validation of dc linearity.

External Calibration Source: Using NIST traceable source and Auto-Cert. routine, the VX2805C will verify internal flash calibration against source and store verification date.

FRONT PANEL LED INDICATORS

MASTER: Green LED. On if unit is configured as the Master in a data collection mode.

CONVERT: Blue LED. On if unit is storing digitized data to internal data memory.

BUSY: Yellow LED. Led blinks when the host computer is accessing via the VXI bus.

STATUS: Red LED. Flashing if unit failed power-on reset diagnostics or if a condition exists that prevents correct unit operation. On for 5 seconds after system reset or power up. Green LED if unit status is OK.

FRONT PANEL CONNECTIONS

INPUTS: 2 each 15-pin "D".

OUTPUTS: Excitation Out, SIPS™ communication, buffered, Analog Out, Ext. Cal. In. Amplimite 50-pin.

EXPANSION CHASSIS CONTROL:

Clk/Trig In: ADC Differential reference clock and trigger input. 8 pin DIN connector.

Clk/Trig Out: ADC Differential reference clock and trigger output. 8 pin DIN connector.

FIFO Control: For start and stop of FIFO.

DAS Start & Stop: For start and halt of SD VXI Modules.

DIGITAL I/O:

Inputs: TTL compatible single ended >1kW, or 100W balanced TTL compatible balanced differential operation.

Outputs: TTL compatible single ended 50W drive or 100W balanced differential operation.

Protection: Buffered ±15V clamp 1A for 2µs or 35VDC.

ACCESSORIES

SIPS™: Smart Interface Panel System.

PIPS™: Passive Interface Panel System.

ENVIRONMENTAL

Operating Temperature: 0 to 30 C

Non-operating Temperature: -20 to 85 C

Non-condensing

PHYSICAL

VXI, single width,"C" size.

Addressing: A16, D16/D32.

Logical Address: Set by Dual HEX-encoded rotary switches for VXI Logical Addressing. Supports Auto LA Assignment.

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